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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,575	04/09/2004	Brian J. Campbell	BP 3242	1894
34399	7590	08/09/2005	EXAMINER	
GARLICK HARRISON & MARKISON LLP			CHANG, DANIEL D	
P.O. BOX 160727			ART UNIT	
AUSTIN, TX 78716-0727			PAPER NUMBER	
			2819	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/821,575	CAMPBELL, BRIAN J.	
	Examiner	Art Unit	
	Daniel D. Chang	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 09 April 2004.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 09 April 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 5, 7, 8, 11, 13, 14, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Sigal et al. (US 5,543,731, “Sigal” hereinafter).

Regarding claim 1, Sigal discloses, at least in Fig. 6, a multiplexer, comprising:

a first logic module (GATE 1) operable to receive a first plurality of data input signals (DATA\_A, DATA\_B) and a first plurality of select signals (SELECT\_A, SELECT\_B) and to generate a first output signal (A) in response thereto;

a second logic module (GATE 2, not shown but similar to GATE 1; col. 3, lines 33+) operable to receive said first set of data input signals and a first set of complementary select signals corresponding to said first set of select signals and to generate a second output signal in response thereto;

an output line (Q) operable to receive a plurality of output signals from said first and second logic modules;

a first gate (inherent transistor in NAND 1) operable to receive said first output signal and to transfer said first output signal to said output line; and

a second gate (another inherent transistor in NAND 1) operable to receive said second output signal and to transfer said second output signal to said output line;

wherein the capacitive loading of said first and second logic modules of each of said data

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input units is isolated from said output line by said first and second gates, respectively (inherent for NAND 1).

Regarding claim 2, Sigal discloses, at least in Fig. 6, that the first and second logic modules comprise static logic (col. 3, lines 12+).

Regarding claim 5, Sigal discloses, at least in Fig. 6 a keeper circuit (LATCH) operable to maintain said output line at a predetermined voltage.

Claims 7, 8, 11, 13, 14, and 17 are essentially the same in scope as claims discussed above and are rejected similarly.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6, 12, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sigal.

Sigal discloses the claimed invention except for the output line not connected to a keeper. It would have been obvious to one having ordinary skill in the art at the time the invention was made to disconnect the keeper from the output line, since it has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. *Nerwin v. Erlichman*, 168 USPQ 177, 179.

Claims 3, 4, 9, 10, 15, and 16, are rejected under 35 U.S.C. 103(a) as being unpatentable over Sigal in view of Horenstein ("Microelectronic Circuits & Devices", 1990 by Prentice-Hall, Inc.).

Lin discloses a multiplexer as discussed above and further discloses a NAND gate (NAND1 in Fig. 6) but does not specifically disclose that the first and second gate comprises a pMOS and an nMOS transistor, respectively.

Horenstein shows a NAND gate having a pMOS and an nMOS transistors.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute the NAND gate of Sigal with the NAND gate of Horenstein. It is an obvious matter of substitution of equivalence.

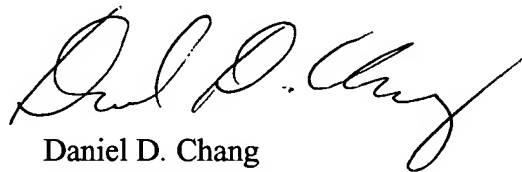
### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel D. Chang whose telephone number is (571) 272-1801. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Daniel D. Chang  
Primary Examiner  
Art Unit 2819

dc

**DANIEL CHANG**  
**PRIMARY EXAMINER**